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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/540,423	06/24/2005	Toshio Kameshima	03500.103610.	9264

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EXAMINER	
ELEY, JESSICA L	

ART UNIT	PAPER NUMBER
2884	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/540,423	KAMESHIMA, TOSHIO	
	Examiner	Art Unit	
	JESSICA L. ELEY	2884	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *32-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *32-46* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 June 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Examiner acknowledges applicant's amendment filed 26 November 2008 which canceled claims 1-31 and added new claims 17-31.

Priority

It is noted that this application appears to claim subject matter disclosed in prior Japanese Patent Application No. 2003-389274, filed on November 19, 2003 and JP 2004-180899 filed on June 18, 2004. ***A reference to the prior application must be inserted as the first sentence(s) of the specification of this application or in an application data sheet*** (37 CFR 1.76), if applicant intends to rely on the filing date of the prior application under 35 U.S.C. 119(e), 120, 121, or 365(c). See 37 CFR 1.78(a).

Examiner politely request applicant amend the specification to place the passages concerning foreign priority in their proper place at the beginning of the disclosure instead of the end.

Response to Arguments

Applicant's arguments filed 26 November 2008 have been fully considered but they are not persuasive.

Applicant argues that Tashiro does not teach the constant current source (e.g., Loas current source) being formed on a signal line at a position on an insulating supporting substrate,

spaced from the readout unit rather than a pixel, and together with the photoelectric converting element or the resetting transistor or the readout transistor, see applicant arguments page 9 paragraph 3. Examiner respectfully disagrees. Tashiro clearly teaches in FIG. 14 the current source formed together with the readout transistor M4, and as detailed in FIG. 11 connected to the signal line at a position on said insulating supporting substrate, spaced from said readout rather than said pixel.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 32, 34, 39-41, 44 and 46 are rejected under 35 U.S.C. 102(b) as being anticipated by Tashiro et al. 20020190215 A1 (henceforth referred to as Tashiro).

Regarding **claim 32**, Tashiro teaches a photoelectric converting apparatus (¶0020) comprising:

an insulating supporting substrate **103 or 104**, comprising:

a pixel comprising a photoelectric converting element **PD** (FIG. 14),

A resetting transistor **M2** having a source and a drain, wherein one of the source and the drain is connected to said photoelectric converting element **PD** and the other of the source and the drain is connected to a resetting power source **RES**,

a readout transistor **M4** having a source, a drain and a gate, wherein the gate is connected to said photoelectric converting element **PD** and one of the source and the drain of said readout transistor is electrically connected to a readout power source,

a signal line **S** connected to said pixel; and

a constant current source (Load current source) connected to said signal line and,

readout unit **N** connected to said signal line,

wherein said constant current source is formed together with the readout transistor M4, and as detailed in FIG. 11 connected to the signal line at a position on said insulating supporting substrate, spaced from said readout rather than said pixel.

Regarding **claim 34**, Tashiro teaches the apparatus of claim 32, as discussed above. Tashiro further teaches said pixel comprises a selecting transistor **M3** connected between the other of the source and the drain of said readout transistor **M4** and the signal line **S**, and said constant current source is formed from amorphous silicon on the same insulating substrate as that of said readout transistor (¶0008).

Regarding **claim 39**, Tashiro teaches the apparatus of claim 34, as discussed above. The apparatus taught by Tashiro utilizes amorphous silicon (¶0005) thus the resetting transistor, readout transistor; selecting transistor and said constant current source are formed in amorphous silicon.

Regarding **claim 40**, Tashiro teaches the apparatus of claim 32, as discussed above. Tashiro further teaches the photoelectric converting apparatus comprising a scintillator (aka

phosphor (¶0004) layer which absorbs a radiation and emits a light of wavelength region detectable by said photoelectric converting element (¶0071).

Regarding **claim 41**, Tashiro teaches the apparatus of claim 32, as discussed above. Tashiro further teaches the photoelectric converting apparatus wherein said photoelectric converting element is a photodiode. Tashiro specify one particular type of photodiode, therefore it would be obvious to one of ordinary skill in the art at the time the invention was made to try using a PIN photodiode or MIS sensor as a person with ordinary skill has good reason to pursue the known options within his or her technical grasp and there are limited number of photodiodes that may be realized in silicon.

Regarding **claim 44**, Tashiro teaches a photoelectric converting apparatus (¶0020) comprising:

an insulating supporting substrate **103/104**, comprising;

a sensor array including a plurality of pixels arranged two dimensionally (FIG. 11), each pixel including a photoelectric converting element **PD** (FIG. 14),

A resetting transistor **M2** having a source and a drain, wherein one of the source and the drain is connected to said photoelectric converting element **PD**, and the other of the source and the drain is connected to a resetting power source **RES**,

A readout transistor **M4** having a source, a drain and a gate, wherein the gate is connected to said photoelectric converting element **PD** and one of the source of said readout transistor and the drain of said readout transistor is electrically connected to a readout power source,

A plurality of signal lines **S** connected electrically and commonly to the others of the sources and the drains of said readout transistors, and

A constant current source (Load current source) connected to said common signal lines; and

A readout unit **N** connected to said signal lines,

wherein said constant current source is formed together with the readout transistor M4, and as detailed in FIG. 11 connected to the signal line at a position on said insulating supporting substrate, spaced from said readout rather than said pixel.

Regarding **claim 46**, Tashiro teaches an X-ray image pickup system (FIG. 24) comprising:

a photoelectric converting apparatus as discussed in claims 32 and 35,

an X-ray generating apparatus **6050;** and

a control unit **6070**,

Wherein said control unit controls operation of the X-ray generating apparatus and the photoelectric converting apparatus (FIG. 24).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 33 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro et al. 20020190215 A1 (henceforth referred to as Tashiro). as applied to claims 32 and 44 above, and further in view of Spivey et al. US 5,528,043 A (henceforth referred to as Spivey).

Regarding **claims 33 and 45**, Tashiro teaches the apparatus of claims 32 and 44, wherein said readout means **M4** includes an amplifier (¶0074) connected to said signal line **SEL1** and an analog multiplexer connected to said amplifier in the form of horizontal and vertical shift registers. Tashiro does not teach the material that the readout unit is made of. Spivey teaches a readout circuit **18** for an X-ray imager is composed of crystalline silicon (C3 L39-42). It would

be obvious to one of ordinary skill in the art at the time the invention was made to form the readout circuit of Tashiro from crystalline silicon since a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp and as demonstrated by the teachings of Spivey one of ordinary skill would have a reasonable expectation of success.

Claims 35, 37 and 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro et al. 20020190215 A1 (henceforth referred to as Tashiro) as applied to claim 17 above, and further in view of Sakuragi US 2001/0033337 A1.

Regarding **claim 35**, Tashiro teaches the apparatus of claim 34 but does not define the components of the constant current source. Sakuragi teaches a constant current source including a transistor of which a gate is connected to a power supply for said constant current source (¶0062). It would be obvious to a person of ordinary skill in the art at the time the invention was made to use the current source taught by Sakuragi as the current source since Tashiro does not disclose the specific elements of the current source thus leading one of ordinary skill to look for teachings as to the specific construction of a current source such as the one taught by Sakuragi, thus leading one of ordinary skill in the art to construct the current source from a transistor of which a gate is connected to a power supply.

Regarding **claim 37**, Tashiro teaches the apparatus of claim 32, as discussed above. Sakuragi teaches the constant current source includes a constant current source transistor in which a gate and a source are mutually connected. It would be obvious to a person of ordinary skill in the art at the time the invention was made to use the current source taught by Sakuragi as

the current source since Tashiro does not disclose the specific elements of the current source thus leading one of ordinary skill to look for teachings as to the specific construction of a current source such as the one taught by Sakuragi, thus leading one of ordinary skill in the art to construct the current source from a transistor of which a gate is connected to a power supply.

Regarding **claim 38**, Tashiro teaches the apparatus of claim 32, as discussed above. Furthermore, neither Tashiro not Sakuragi expressly teach connecting the gate and the source of the transistor in the constant current source by a resistor. However it would be obvious to one of ordinary skill in the art at the time the invention was made to use a resistor in this instance in order to bias any offset voltage that may occur.

Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro et al. 20020190215 A1 (henceforth referred to as Tashiro) and Sakuragi US 2001/0033337 A1 as applied to claim 35 above, and further in view of NPL ELE343 Lab, Transistor modeling http://www.ele.uri.edu/Courses/c;e343/lan/lab0/index.html (henceforth referred to as ELE343).

Regarding **claim 36**, the teachings of Sakuragi regarding the use of a transistor as part of a constant current do not specify the relationship between the voltage of the drain-source, gate-source, and threshold voltage. However, the standard teachings in the art imply that the relation would be Vds > Vgs –Vth in order to result in a device that provides a constant current source, see page 3 of ELE343. Thus it would be obvious to a person of ordinary skill in the art at the time the invention was made to use the relation Vds > Vgs -Vth, in which Vds is a drain-source

voltage, Vgs is a gate-source voltage and Vth is a threshold voltage for the current source of Sakuragi as this is necessary for standard operation of a transistor.

Claims 42 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Tashiro et al. 20020190215 A1 (henceforth referred to as Tashiro) as applied to claim 32, and and in further view of Kameshima et al. US 20010033336 A1 (henceforth referred to as Kameshima.

Regarding **claims 42 and 43**, the detector taught by Tashiro and Sakuragi do not use direct conversion photoelectric converting elements. However, such elements are well known in the art. For example Kameshima teaches direct conversion when waves such as X-rays are being detected, using materials such as amorphous selenium, lead (II) iodide, and gallium arsenide (¶0026). It would be obvious to one of ordinary skill in the art at the time the invention was made to use the direct conversion element taught by Kameshima as the photoelectric converting element in Tashiro as this negate the need for an additional scintillation layer.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JESSICA L. ELEY whose telephone number is (571)272-9793. The examiner can normally be reached on Monday - Thursday 8:00-6:30 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Dave Porta can be reached on (571) 272-2444. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/David P. Porta/
Supervisory Patent Examiner, Art Unit 2884

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Examiner, Art Unit 2884